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ABSTRACT

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This paper discuss on the modeling and simulation of Silicon Nano Wire field Effect Transistors (SiNW FETs). Modeling and simulation of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is very essential in order to understand the device physics, electrostatics and other important phenomena occurring in this device. Therefore, the modeling is done assuming both ballistic transports. The modeling of SiNW FETs assuming ballistic transport is an extension of the Natori's theory of ballistic MOSFETs. After the derivation of the model, its benchmarking is also done. This is accomplished by comparing the simulation results of the developed model, which is implemented using MATLAB, with numerical simulation results. Various important parameters are extracted and used for comparison. The comparison shows that there is a good agreement between the simulation results of developed model and numerical results of simulation.

Key words: *Nanowire (NW), Sillicon NW Field Effect Transistor, benchmarking, Ballastic MOSFET*

INTRODUCTION

There has been great interest with the invention of Carbon Nanotube by Iijim (Wan *et al.* 2009) in the preparation and characterization of other one dimensional (1D) structures that refers to naowire (NW) nanorods and nanobelts (Rao and Govindaraj, 2005). By the recent experimental analysis inorganic nanowire can be used as a active components in devices. Nanowires of various inorganic materials have been synthesized and characterized in the last four to five years. A NW is an object with a 1D aspect in which the ratio of the length to the width is greater than 10 and the width does not exceed a few tens of nanometers (Wiederrecht 2010). In the recent moment, this definition has been expanded to atomic and molecular wires, which have proved to exhibit very interesting physical properties without necessarily having the geometrical properties, defined earlier. NWs represent the smallest dimension for efficient transport of electrons and excitons. They will be used as interlinks and critical devices in nanoelectronics and nano-optoelectronics (Rao and Govindaraj, 2005). They are very much attractive for nano-science studies and for nanotechnology applications. NWs, compared to other low dimensional systems, have two quantum confined directions, while still leaving one unconfined direction for electrical conduction (Seoane *et al.* 2009). Now a days, different types of NWs are being analyzed and are being fabricated.

Despite the different types of semiconductor NWs have been analyzed, Silicon Nanowires have become prototypical nanowires. This is for the reason, they can be easily prepared, Si/ SiO2 interface is chemically stable, and SiNWs are used in a number of device demonstrations that have well-known silicon technology-based counterparts (Richter *et al.* 2008). The nanowire transistor has the potential to overcome the problems due to SCEs in SOI MOSFET and has gained significant attention from both device and circuit developers. The effective suppression of SCEs due to the improved gate strength, themulti-gate SiNW FETs show excellent current drive and have the merit that they are compatible with conventional CMOS processes (Dattoli 2010). Semiconductor NWs are emerging as a powerful class of materials that, through controlled growth and organization, are opening up novel opportunities for nanoscale electronic and photonic devices. SiNWs have been demonstrated as one of the promising building blocks for future nano-devices such as FETs, solar cells, sensors and lithium battery (Wan *et al.* 2009).

MATERIALS AND METHODS

The compact modeling for SiNW FETs is developed and described together with the theoretical back ground. The model is divided into two parts, namely, a modeling approach which assumes ballistic transport and that assuming transport in the presence of scattering. The former part is developed based on Natori's theory of ballistic MOSFETs and modified to include two dimensional effects. The latter part is based on McKelvey's flux theory. We begin by describing the basic Natori's model for ballistic transport in the first section and proceed to the model derivation. In the second section, we will derive our model for transport in the presence of scattering.

Sillicon Nano-wire Field Effect Transistor

Nano-wire field effect transistors (NWFET) have been proposed and now studied by many research groups around the world. This isbecause, they are promising candidate to sustain the relentless progress in scaling for CMOS devices (Cao 2004). Several key factors have contributed to the boom of NW research. First, semiconductor NWs can be prepared in high-yield with reproducible electronic properties as required for Large Scale integrated (LSI) systems. Second, compared with "top–down" nanofabricated device structures, "bottom–

up" synthesized NW materials offer well controlled size; that is at or beyond the limits of lithography. In addition, the crystalline structure, smooth surfaces and the ability to produce radial and axial NW hetero structures can reduce scattering. These results in higher carrier mobility compared with nanofabricated samples with similar size. Finally, the body thickness (diameter) of NWs can be controlled down to well below 10 nm. Therefore, electrical integrity of NW-based electronics can be maintained even as the gate length is aggressively scaled. This is a feature that has become increasingly difficult to achieve in conventional MOSFETs (Wolf 2006). GAA SiNW FETs have attracted significant interest because of their excellent electrostatic integrity even at the nanoscale. Various types of SiNW FETs are being explored as a promising candidate for future transistors replacing planar MOSFETs in logic and Dynamic Random Access Memory(DRAM) applications, and their fabrication is being studied either from top-down or bottom-up approaches (Lundstrom and Guo, 2006).

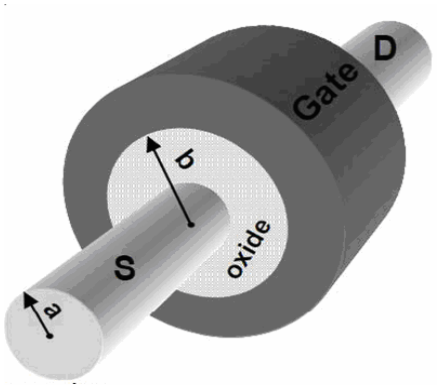

Fig. 1. Sillicon Nano-wire Field Effect Transistor

Modeling of SiNW FET

The model derivation begins by describing the different directed moments describing the ballistic transport of NW FETs. According to Natori's theory of ballistic MOSFETS, the directed moments to be evaluated in order to derive the important parameters of the SiNW FET are (Colinge 2008). The electron concentration at the top of the barrier, populated according to the source Fermi level $n_L^+(0)$ given by

$$n_L^+(0) = \frac{1}{L}\sum_{k>0} f_0(E_f)$$

The electron concentration at the top of the barrier, populated according to the drain Fermi-level, $n_L^-(0)$ is given by:

$$n_L^-(0) = \frac{1}{L}\sum_{k<0} f_0(E_f - qV_D)$$

The positive directed current due to source injection, given by:

$$I^+ = \frac{1}{L}\sum_{k>0} qvf_0(E_f) = qn_L^+(0)v^+(0)$$

The negative directed current due to drain injection, I-, given by:

$$I^- = \frac{1}{L}\sum_{k<0} qvf_0(E_f - qV_D) = qn_L^-(0)v^-(0)$$

Assuming a simple parabolic energy band structure and also assuming that only on sub-band is occupied, the directed moments are evaluated to give (Colinge 2008).

$$n_L^+(0) = \frac{N_{1D}}{2}F_{-\frac{1}{2}}(\eta_F)$$

$$n_L^-(0) = \frac{N_{1D}}{2}F_{-\frac{1}{2}}(\eta_F - U_D)$$

$$I^+ = \frac{qk_BT}{\pi hbar}F_0(\eta_F)$$

$$I^- = \frac{qk_BT}{\pi hbar}F_0(\eta_F - U_D)$$

Describing the positively populated electron concentration, $n_L^+(0)$, negative populated electron concentration,

$$\eta_F = \left(\frac{E_F - \varepsilon_1(0)}{K_BT}\right)$$

$$U_D = \frac{qV_D}{k_BT}$$

$$V_T = \sqrt{\frac{2K_BT}{\pi m^*}}$$

N_{1D} is the 1D effective DOS given by

$$N_{1D} = \sqrt{\frac{2m^* K_B T}{\pi hbar^2}}$$

F0 and F-1/2 are the Fermi-Dirac integrals of 0 and -1/2 order respectively. The Fermi-Dirac integral of any order is generally defined as.

$$F_j(\eta_F) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{\varepsilon^j d\varepsilon}{1+\exp^{(\varepsilon+\eta_F)}}$$

Where, Γ. is the gamma function. The Γ. function is just the factorial when its argument is a positive integer for an integer n,

$$\Gamma(n) = (n-1)!$$

$$\Gamma\left(\frac{1}{2}\right) = \sqrt{\pi}$$

$$\Gamma(p+1) = p\Gamma(p)$$

Throughout this chapter, we will use these equations for the derivation of the current and charge density equations of SiNW FET. Assuming 1D electrostatics and neglecting 2D electrostatics, the gate voltage is the sum of the surface potential and the voltage drop across the oxide:

$$V_G = \psi_s - \frac{Q}{C_{ox}}$$

Substituting the expressions for the surface potential and the charge density at the top of the barrier Equation 3.17 becomes*:*

$$V_G = \frac{\varepsilon_1(0)}{q} - \frac{q\eta_L}{C_{ox}}$$

After solving Equation 3.18 for $\varepsilon_1(0)$ we get:

$$\varepsilon_1(0) = qV_G + \frac{q^2\eta_L}{C_{ox}}$$

$n_L^-(0)$, the positive directed current, I^+ , and the negative directed current, I^- respectively.

Modeling of the Gate Capacitance

Before further continue the derivation, the expression for the oxide capacitance, Cox, is derived first. The SiNW FET structure. It is a FET having a cylindrical NW as a channel. This configuration gives the highest performance of the NW transistor because of the strong control of SCEs. Because the NW transistor has a cylindrical cross section, its capacitance can no longer be calculated using a simple parallel-plate model. The capacitance C of the capacitor is defined, in general, as the ratio of the magnitude of the charge on one of the plates to the potential difference between them (Colinge 2008) that is,

$$C = \frac{Q}{V} = \frac{\varepsilon \oint E.ds}{\int E.dL}$$

Using above equation, C can be obtained for any given two-conductor capacitance by following either of these methods

1. Assuming Q and determining V in terms of Q (involving Gauss's law)
2. Assuming V and determining Q in terms of V (involving solving Laplace's Equation)

The former method is used here and it involves taking the following steps:

1. Choose a suitable coordinate system.

Let the two conducting plates carry charges + Q and - Q. Determine E using Coulomb's or Gauss's law and find V from $V = -\int E.dl$ The negative sign may be ignored in this case because we are interested in the absolute value of V. Finally, obtain C from C = Q/V (Mattew 2007) Fig. 1 Illustration of a SiNW FET; the gate stack is wrapped around the semiconductor NW; a is the radius of the NW (Colinge 2008) Considering the inversion charge in the NW can be approximated by a charge sheet on the outer surface of the wire. The charge on the gate is on the inner wall of the gate electrode. The capacitance can be obtained by calculating the voltage drop across the gate oxide.

The charge per unit length at the surface of the wire is given by:

$Q = \varepsilon \oint E.ds = \varepsilon E_\rho 2\pi\rho$ Where, for an infinite line charge if we apply Gauss's law to an arbitrary length l of the line: $\rho_l l = Q = \oint D.ds = D_\rho \oint ds = D_\rho 2\pi\rho l$

where, ρ is the radius of the NW and $ds = 2\pi\rho l$ is the surface area of the Gaussian surface, we get

$$E = \frac{Q}{2\pi\rho l} a_\rho$$

Neglecting flux fringing at the cylinder ends,

$$V = -\int_1^2 E.dl = -\int_a^b \left[\frac{Q}{2\pi\varepsilon\rho L} a_\rho\right] d\rho a_\rho$$

$$V = \frac{Q}{2\pi\varepsilon L} \ln\frac{a}{b}$$

Thus the capacitance of the cylindrical NW is given by:

$$C = \frac{Q}{V} = \frac{2\pi\varepsilon L}{\ln\frac{b}{a}}$$

Where, a is the radius of the NW and b is given by: b = a + tox. Where, tox is the thickness of the insulator. Finally, the capacitance per unit length of the NW is given by:

$$\frac{C}{L} = \frac{2\pi\varepsilon}{\ln\frac{b}{a}}$$

Above indicates the effective gate capacitance of the NW transistor is a function of the NW radius as well as the gate oxide thickness. This relationship can be exploited to reduce the effective gate oxide thickness without using higher k dielectric. Having derived the capacitance of the insulator for the cylindrical NW FET, let's proceed to the derivation for the other parameters and enters in to the equation of charge and current, its expression is derived here. We get energy for the first sub-band $\varepsilon_1(0)$

$\varepsilon_1(0) = E_F - \eta_F k_B T$ Substituting the value of $\varepsilon_1(0)$ and assuming 1D electrostatics of

$$\eta_F = \frac{E_F - qV_G}{k_B T} - \frac{q^2 n_L(0)}{k_B T C_{ins}}$$

Modeling of the Drain Current:

The drain current is the difference between the positive and negative going currents I^+ and I^- respectively. therefore, the drain current for a SiNW FET (Kidist Moges 2011).

$$I_D = I^+ - I^-$$

$$I_D = \frac{2qk_B T}{h}\left\{F_0(\eta_F) - F_0(\eta_F - U_D)\right\}$$

$$I_D = I_0\left\{F_0(\eta_F) - F_0(\eta_F - U_D)\right\}$$

Where, $I_0 = \frac{2qk_B T}{h}$

RESULTS AND DISCUSSION

The linear transfer characteristics drawn from the compact modeling simulation and that of the numerical simulation are shown in Figures 2(a) and 2(b) respectively. From these graphs the ON state current is extracted. The value of Ion for both simulations is taken as the current at zero gate voltage and at the highest drain voltage, which in this case is 0.8 V.

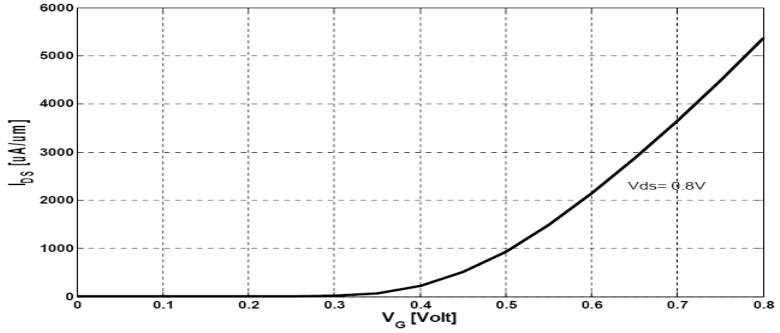

Fig. 2(a) Compact Modelling

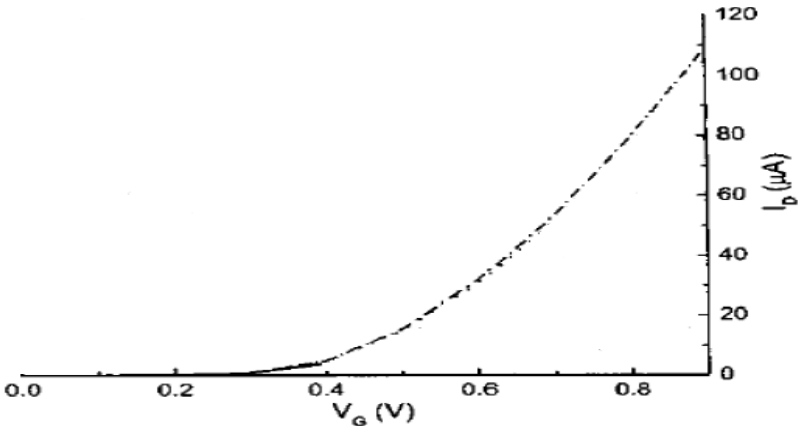

Fig. 2(b) Numerical Simulation

Fig. 2. The linear transfer characteristics from (a) the compact modeling simulation and (b) from the numerical simulation

From the compact modeling simulation, the on-state current is calculated to be 4950 mA/μm. Also the on-state current from the numerical simulation is calculated to be 5024 mA/μm, which is a little bit higher than that from the compact model. This implies there is a very good agreement in the value of Ion between the two simulation results.

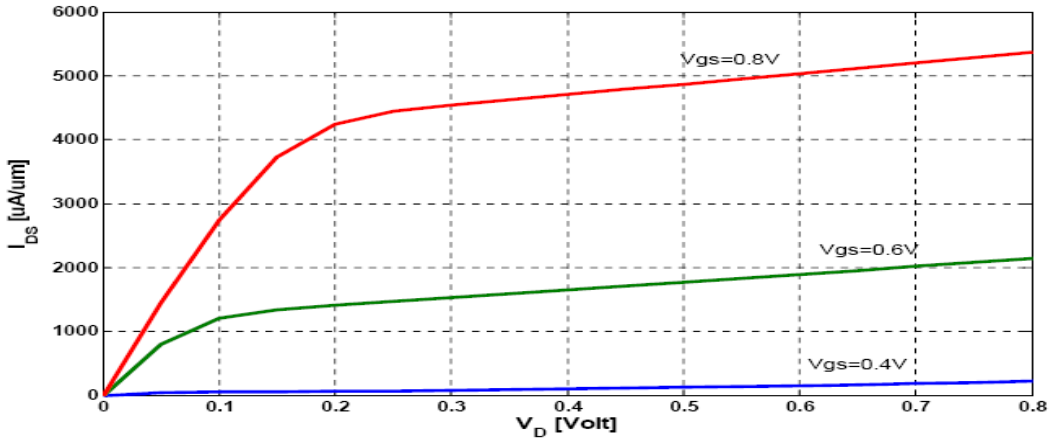

Fig. 3(a) Compact Modelling

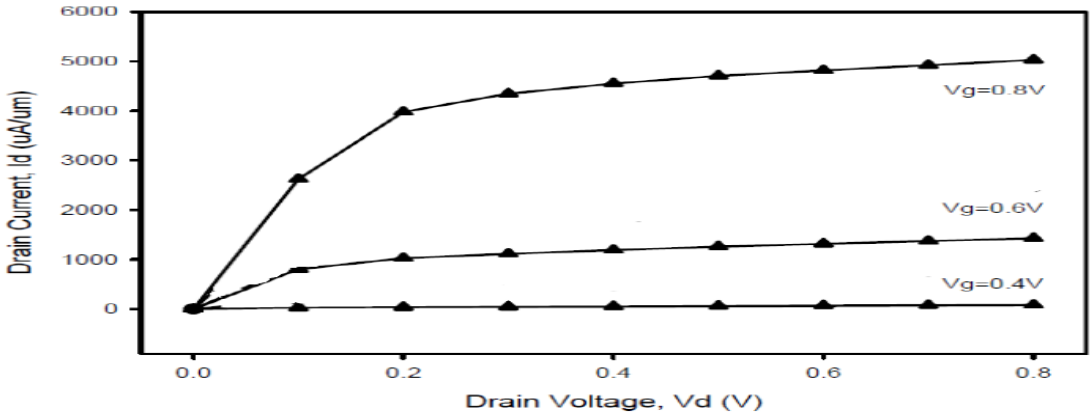

Fig. 3(b) Numerical Modelling

Fig. 3. Simulated Ids – Vds curves for the SiNW FET from (a) compact modeling simulation. (b) Numerical modeling simulation

Finally, the out put characteristics curves, I_{ds} - V_{ds}, drawn from the compact modeling and from that of the numerical simulation are shown in Figures 3(a) and 3(b). Transconductance is the most important dynamic parameter of MOS for analogue applications because it reflects the transfer efficiency from input to output. The output conductance is extracted from these graphs for a gate voltage of 0.8 V. The output resistance is found to

be 147.17 kΩ from the compact modeling simulation result and 187.46 kΩ from the numerical simulation result. In both cases a very high output conductance is found and they are in good agreement.

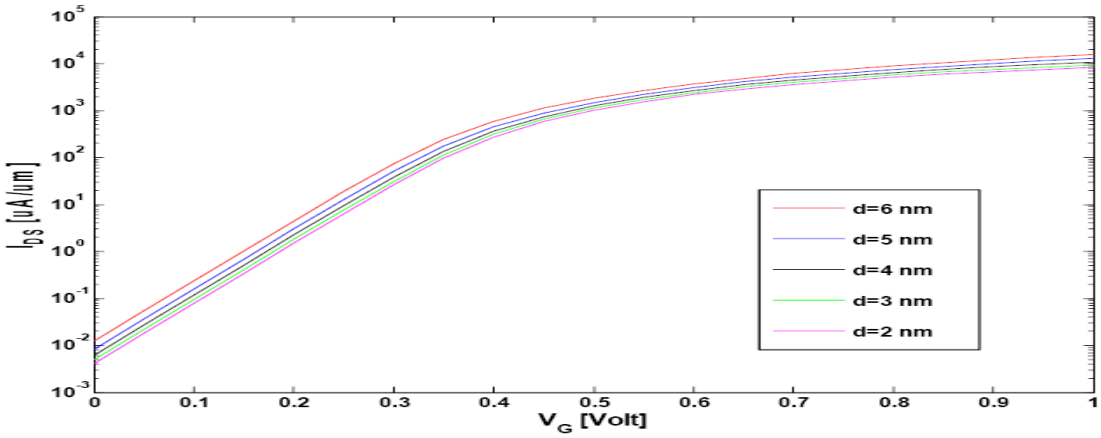

Fig. 4. Log Ids –Vgs graph with varying diameter from 2 nm to 6 nm in steps of 1nm

For all simulations, the gate oxide thickness is kept at 1 nm and the NW diameter is varied from 2 nm to 6 nm. The voltage range taken for the gate and drain bias is 0 V-1 V. It is known that a high performing transistor should have a reasonably low Off-state current and a large On-state current, so that its Ion / Ioff ratio becomes fairly large. As we can see from Figure 4, the value of Ioff decreases with decreasing NW diameter. This is due to the high suppression of SCEs because of the greatest control of gate over the channel. Therefore, as expected, gate has the greatest control of the channel for lower NW diameters.

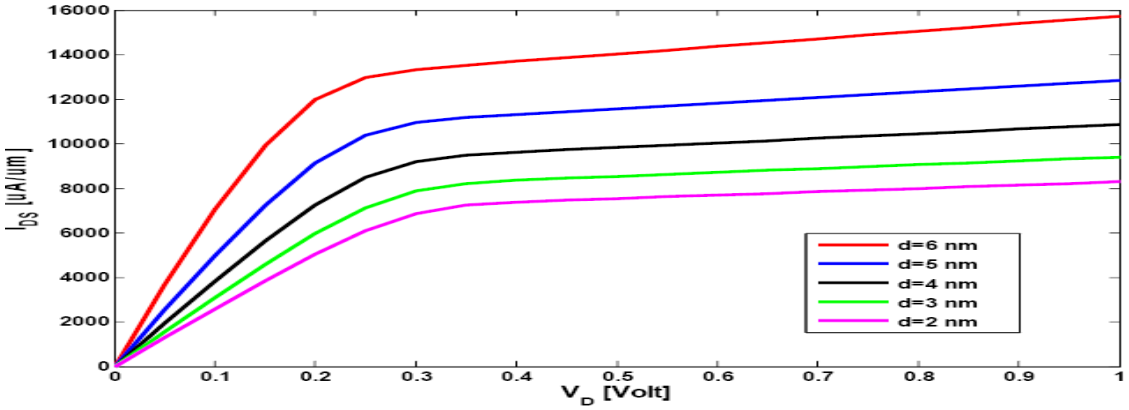

Fig. 5. Ids-Vds characteristics graph for varying diameters from 2 nm to 6 nm in steps of 1nm

Figure 5 shows the output, Ids-VD, characteristics graph with varying NW diameters. The drain supply voltage is kept at 1 V for all simulations and the gate supply voltage is varied b/n 0V and 1Vin the simulation. From this graph, we can see that the highest current occurs at the highest NW diameter taken in the simulation. One possible reason for the increase of current with the NW diameter can be the quantum confinement effect. As the NW diameter decreases there will be quantum mechanical confinement of states which decreases the On-state current. Figure 3 depicts Ids-Vds characteristics with varying NW diameter.

CONCLUSION

In conclusion, the modeling of SiNW FETs is done. The model development was divided into two sections. The first section is devoted to the modeling of SiNW FETs assuming ballistic transport. The model is based on Natori's theory of ballistic MOSFETs and is extended to include 2D electrostatic effects. The simulation results found from the developed model were compared with that of the numerical simulation results. The numerical simulation results were found from the NanoHub, using the software, NW. The comparison results give a good agreement which shows the accuracy of the developed model.

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